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~~Description~~

Method for modulating a basic clock signal for digital circuits and clock modulator for implementing the method

The invention relates to a method for modulating a basic clock signal for digital circuits and a clock modulator for modulating a basic clock signal for digital circuits. Modulation of the basic clock signal is used in order to give interference caused by the basic clock signal a broader-band configuration and thus to distribute the interference energy between additional frequencies and hence to reduce the absolute heights of the resulting interference spikes.

The applicant's patent application (DE 198 02 065.1), which is a prior application, discloses a method for modulating a basic clock signal for digital circuits and a corresponding clock modulator in which the distances between adjacent switching edges are altered, the respective distance being achieved by virtue of the fact that the basic clock signal is conducted via a changing number of delay units and the distances between the adjacent switching edges are altered in this way.

This method and this clock modulator have the disadvantage that frequency modulation is achieved which, although it greatly attenuates the fundamental frequency, does not readily correspond to the fundamental frequency in terms of its time average.

The object of the invention, therefore, is to ~~specify~~ provide a method for the frequency modulation of a basic clock signal which outputs a modulated clock signal which is identical on average to the basic clock signal, and a corresponding clock modulator for implementing the method.

The object is achieved for a method ~~by virtue of the fact that~~ the delay times of the delay units are calibrated, the delay units each having a plurality of delay elements and the delay elements being connected in or out individually and/or in groups. This makes it possible to compensate for effects such as, for example, current operating temperatures, changes in the voltage supply and ageing-dictated changes. This calibration is configured in a particularly simple manner if the delay elements are connected in or out in a stepwise approximated manner.

This calibration can be carried out particularly rapidly and with always the same number of steps if firstly, during a coarse calibration, the same number of delay elements is connected in or out in each case in all the delay units and then, in a fine calibration, a respective delay element in one or more delay units is connected in or out.

One ~~possibility for~~ manner of determining the distances between the switching edges may be realized by cyclically recurring random numbers, from which the respective distance is derived.

The selection of the random numbers becomes particularly simple if the random numbers are inverted after n cycles for n cycles and the inverted numbers are then used for deriving the switching edges. The effect achieved as a result of this is that even given an unfavorable selection of the random numbers used, the modulated frequency on average corresponds to the

fundamental frequency. This makes it possible, for example, to use the modulated frequency to provide an accurate time base for a clock, for example.

By virtue of the fact that the switching edges are derived not only as a function of the random number but also as a function of a modulation factor, it is possible to realize different modulation factors.

One manner of ~~possible~~ determination of the next switching edge can be implemented by the formula specified herein ~~in claim 7~~. This makes it possible to freely select the modulation factor, the number of delay elements and of different random numbers or switching edges within the scope of the physical limits of the clock signal to be modulated and of the switching device.

It is also possible to assign a specific distance between the switching edges to each random number as a function of the modulation factor, the clock signal to be modulated and the switching device, to store these values in a memory and to read them out and use them as required.

A clock modulator according to the invention has a number of series-connected delay units with adjustable delay times between which taps are arranged, so that the basic clock signal can be conducted via a changing number of delay units and the distance between the switching edges can be altered in this way, the adjustability of the delay units being realized by virtue of the fact that the delay units are each constructed from a plurality of delay elements which can be connected and disconnected individually.

By virtue of the fact that the delay times of the delay units are adjustable, overall the clock modulator can be used for different fundamental frequencies and modulation factors.

The selection of the random numbers becomes simple by virtue of an inverting device for inverting the random numbers. This inverting device can be connected in after n cycles of the random numbers and can be disconnected again after a further n cycles. As long as the random numbers are inverted, the inverted random numbers, instead of the random numbers, are used for deriving the distances between adjacent switching edges. The effect achieved as a result of this is that the average clock duration of the modulated frequency is equal to the duration of the modulated basic clock signal, irrespective of the selection of the random numbers.

The invention is explained in more detail below using exemplary embodiments.

In the ~~figures~~:

Figure 1 shows a diagram containing the basic clock signal and the generation of the modulated clock signal,

Figure 2 shows a block diagram of a possible exemplary embodiment,

Figure 3 shows an exemplary embodiment of a particularly preferred clock modulator,

Figure 4 shows a function diagram of the exemplary embodiment from Figure 3,

Figure 5 shows a block diagram of an exemplary embodiment of a delay unit, and

Figure 6 shows a possibility for approximated calibration of series-connected delay units.

Figure 1 shows an unmodulated basic clock signal CL, whose half-periods T_0 are divided into 6 respective sections having the length t = 1. A random number generator supplies 5 different random numbers Z 0 to 4 in periodic cycles. The distances between the individual switching edges of the clock signal to be modulated are determined depending on the random number Z and the modulation factor K. Thus, in the case of the middle random number (2), the distance between the adjacent switching edges amounts to a half-period T_0. Given a modulation factor of 1, the following distances between the switching edges result for the remaining random numbers:

0 = 4t
1 = 5t
3 = 7t
4 = 8t

For a modulation factor of 2, the following result for the random numbers:

0 = 2t
1 = 4t
3 = 8t
4 = 10t

One possibility for calculating the respective next switching edge SF is afforded by the following equation 1:

$$a_{i+1} = (a_i + p - \left(\frac{N-1}{2} - Z_{i+1}\right)K) \bmod p = X \bmod p \qquad (1)$$

The following furthermore results:

x = l * p + a x*t

where l is the interval in which the next switching edge lies, p is the number of possible switching points per half-period T_0 and a is the position of the switching edge in the corresponding interval.

The calculation of the switching edge of the modulated clock signal CM 1 with the modulation factor 1 produces the following for the random number 1 at the beginning of the last switching edge SF 0 with the position a = 0 in the interval 0:

$$a_{i+1} = (0 + 6 - \left(\frac{5-1}{2} - 1\right) \times 1) \bmod 6 = 5 \bmod 6$$

$$5 = l * 6 + 5 * 1$$

from this it follows that:

l = 0 a = 5

This states that the switching edge SF 1 lies in the same interval at a = 5. If l = 1, the next switching edge lies in the next interval; at l = 2, the switching edge lies in the next interval but one.

The following results for the switching edge SF 2:

$$a_{i+1} = (5 + 6 - \left(\frac{5-1}{2} - 4\right) * 1) \bmod 6 = 13 \bmod 6$$

$$13 = l * 6 + a * 1$$

l = 2 a = 1

This means that the switching edge SF 2 lies in the next interval but one given the value a = 1.

The following results for the switching edge SF 3:

$$a_{i+1} = (1 + 6 - \left(\frac{5-1}{2} - 2\right) * 1) \bmod 6 = 7 \bmod 6$$

$$7 = l * 6 + a * 1$$

l = 1 a = 1

The following results correspondingly for the switching edge SF 4:

$$a_{e+1} = (1 + 6-\left(\frac{5-1}{2} - 0\right) * 1)\text{mod}6=5\text{mod}6$$

$$5 = l * 6 + a * 1$$

$$l = 0 \quad a = 5$$

This means that the switching edge SF 4 lies in the same interval at the location 5.

For the clock signal CM 2 with the modulation factor 2, the following result for the switching edges SF 6 to SF 9:

For the switching edge SF 6:

$$a_{i+1} = (0 + 6-\left(\frac{5-1}{2} - 1\right) * 2)\text{mod}6=4\text{mod}6$$

$$4 = l * 6 + a * 1$$

$$l = 0 \quad a = 4$$

For the switching edge SF 7:

$$a_{i+1} = (4 + 6-\left(\frac{5-1}{2} - 4\right) * 2)\text{mod}6=14\text{mod}6$$

$$14 = l * 6 + a * 1$$

$$l = 2 \quad a = 2$$

For the switching edge SF 8:

$$a_{i+1} = (2 + 6-\left(\frac{5-1}{2} - 2\right) * 2)\text{mod}6=8\text{mod}6$$

$$6 = l * 6 + a * 1$$

$$l = 1 \quad a = 2$$

For the switching edge SF 9:

$$a_{i+1} = (2 + 6-\left(\frac{5-1}{2} - 0\right) \times 2)\text{mod}6=4\text{mod}6$$

4 = 1 * 6 + a * 1

1 = 0 a = 4

The block diagram of an exemplary embodiment of the clock modulator according to the invention in Figure 2 has n series-connected delay units D_1 to D_n with upstream and downstream taps A_0 to A_n connected to a multiplexer 1. The individual delay units D_1 to D_n each generate a delay having the length $t = \frac{2T_0}{n}$ with the result that the complete delay series delays the unmodulated basic clock signal CL present at the input 6 by a total of one period. A calibrating device 2 compares the basic clock signal CL present at the input E with the signal present at the output A_n of the last delay element D_n. If the instants of the switching edges of the two signals do not correspond, the calibrating device 2 calibrates the delay units D_1 to D_n in such a way that the two signals correspond.

m random numbers are generated cyclically with the aid of a feedback shift register 3.

Different random number sequences can be selected by means of an initialization device 4.

As soon as one cycle of the random numbers has ended, during the subsequent cycle the random numbers read from the feedback shift register are inverted by an inverter 5, in order to obtain uniform distribution of the random numbers and thus of the different delays. If there are an even number of different random numbers, said number is reduced by one in a map device 6, thereby producing an odd number of different random numbers. This reduction can be realized for example as follows: when the highest random number is present, it is not taken, rather the remaining random numbers are taken one after the other. This can be done for example as follows: when said highest random number is present,

a counter which counts from zero up to the highest random number still allowed is read and is then incremented by one.

The random numbers thus obtained are used, as described above with reference to Figure 1, in the arithmetic unit 7 in order to determine the tap A_0 to A_n to which the multiplexer 1 must be switched so that the switching edge corresponding to the random number and to the modulation factor is obtained.

In Figure 3, 7 delay units D_1-D_7 are connected in series to form a delay chain via which the basic clock signal CLK is conducted. The basic clock signal CLK (corresponding to the signal TAPP0) and the signals TAPP1-P3 which leave the delay units D_1-D_3 are respectively present at an input 20a-d of a multiplexer 20, and the signals TAP N0 - N3 which leave the delay units D_4-D_7 are present at a respective input 21a-d of the multiplexer 21. The outputs of the multiplexers 20, 21 are connected to the inputs of a multiplexer 22, whose output is connected to the input of a toggle flip-flop 23, at whose output the modulated clock signal f_{MOD} is present.

In addition, the signals TAPP0 - TAPP3 are also passed to a calibrating unit 24, which monitors whether the delay of said signals is correct. If this is not the case, the delay units D_1-D_4 are calibrated until the delay is correct. The values determined for delay units D_1-D_4 are also accepted for the delay units D_5 to D_7, since they have the same operating parameters as the delay units D_1-D_4, particularly if all the delay units D_1-D_7 or even the entire clock modulator are integrated in an IC. This calibration may be effected continually or at specific time intervals or, by way of example, may be carried out in the event of changes in specific parameters such as, for example, temperature or circuit.

Figure 3 furthermore shows a multiplier 25, two adders 26, 27, a register 28, a toggle flip-flop 29, a lock flip-flop 30 and a random number generator 31.

Equation 1 can be rewritten as follows:

$$S = a_{i+1} = (a_i + K * Z_{i+1} + c) \text{ modp}$$

where c = p-((N-1):2)*K

The next random number Z_{i+1} is present at the input 25a, the modulation factor K is present at the input 25b, the constant c is present at the input 26a and the position a_i of the preceding switching edge SF, which is read from the register 28, is present at the input 26b. The product from the multiplier 25 and the sum from the adder 26 are summed in the adder 27 to give a sum S. The highest bit of this sum S is passed to the set input of the lock flip-flop 30, the second highest bit is passed to the input of the toggle flip-flop 29, and the two remaining, lower bits are passed to the register 28. The output of the register 28 drives the two multiplexers 25, 26 and is furthermore fed back to an input of the adder 26.

Figure 4 shows an exemplary illustration of the method of operation of the above-described clock modulator in the form of a diagram. In this case, TAPP0 to TAPP3 denote the signals which are present at the inputs of the multiplexer 20, and TAPN0 to N3 the signals which are present at the inputs of the multiplexer 21. LB denotes the number produced by the lowest two bits of the sum S and thus represents the number of the signal TAPP0-TAPP3 and TAPN0-TAPN3, Z_i denotes the random number which is present in each case, UB denotes the number of the two upper bits of the sum S, INT denotes the output of the toggle flip-flop 29, and LOCK denotes the output of the lock flip-flop 30.

Suppose that the number of possible random numbers Z is = 3, namely 0, 1 and 2, the number of possible switching points p per half-period T_0 is 4 (namely in each case the rising edge of TAPP0 to P3 and TAPN0 to N3) and the modulation factor is K = 1.

Consequently, the sum S may have values of from 3 to 8, written digitally:

	UB	LB
3	00	11
4	01	00
5	01	01
6	01	10
7	01	11
8	10	00

The modulation begins with the value 3 in the register 28, the random number Z_i = 1 and the outputs of the flip-flops 29, 30 shall be at 0. If the value 0 is present at the input of the multiplexer 22, the latter switches through to the multiplexer 20, and to the multiplexer 21 in the case of the value 1. The 3 means that the input TAPP3 and respectively TAPN3 of the multiplexers 21 is switched through, with the result that the signal which is present downstream of the delay unit D3 is switched through, which signal, upon its next positive edge, will switch over the output of the toggle flip-flop 23.

The next input to be switched through, which is calculated in parallel with this:

$$S = 3 + 1 \times 1 + 3 = 7 \text{ or, in binary, } 0\ 1\ 1\ 1$$

is accepted into the register 28, the toggle flip-flop 29 and the lock flip-flop 30 with the next positive edge of the signal ST which leaves the multiplexer 22.

Consequently, the lower two bits UB = 11 = 3 and the upper bits exhibit 01 = 1. A 3 is thus present in the register 28, with the result that the inputs TAPP3 and TAPN3 are switched through; the second highest bit is a 1, with the result that the toggle flip-flop 29 changes over its output, to be precise from 0 to 1, with the result that the signal at the output of multiplexer 21 is switched through. Consequently, the positive edge of TAPN3 switches the toggle flip-flop 23 to 0 again. The further calculation proceeds correspondingly. If the sum S = 8, digitally 1000, the lock flip-flop 30 inhibits the toggle flip-flop 23, with the result that it cannot change its output.

Figure 5 reveals the possible structure of a delay unit D. The delay unit D comprises m series-connected delay elements 10. The delay elements 10 each have a clock input 11, two clock outputs 12, 13 and a control input 14. The respective clock output 12 is connected to the output 14 of the delay unit D, while the respective clock output 13 is connected to the clock input 11 of the respectively succeeding delay element 10. The control inputs 14 determine the clock output 12, 13 at which the (delayed) clock signal is present and thus whether the clock signal is to be delayed further or is to pass undelayed to the output 14. Consequently, the delay time of each delay unit D can be varied in a wide range.

The timing diagram in Figure 6 shows one possibility for approximated calibration of the delay units from Figure 3. Firstly, in the first cycle C1, the same number of delay elements are used in each delay unit D1-D4 in order to delay the clock signal CL. Since the clock signal is delayed by more than one complete half-period in the case of the delay unit D4, an identical number of delay elements are in each case connected out in the delay units D1-D4. This is carried out in a plurality of steps with a decreasing number

until, by connecting in or out a respective delay element in each delay unit, the clock signal is delayed by almost half a period in the case of the delay unit D4 and the end E of the coarse calibration is reached. Then, during the fine calibration, individual delay elements in a few or one delay unit are connected in or out until, in the penultimate step Cn-1, the clock signal is delayed by more than half a period in the case of the delay unit D4, so that then, in the last step Cn, by connecting out a delay element, the series of delay units have been calibrated in such a way that, in the case of the delay unit D4, the clock signal is shortened by less than the time duration of the delay of a delay element shorter than half a period of a clock signal.

The delay units D5-D7 are then set in a corresponding manner.

It is also possible to calibrate all the delay units D1-D7 simultaneously if a further delay unit (not illustrated) is also arranged downstream of the delay unit D7 and the delay units are calibrated in the manner described above until, as a result of delay elements having been connected in or out, the clock signal at the output of the delay unit which is not illustrated is delayed by the duration of a complete period.